THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte RUBY BEI-LOH LEE and JOHN P. BECK

_____

Appeal No. 95-3497
Application 08/158,649[1]

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ON BRIEF

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Before HAIRSTON, MARTIN, and CARMICHAEL, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 3, 5-14, and 16-20 under 35 U.S.C. § 103.[2] Claims 4 and 15 stand rejected for depending from

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[1] Application for patent filed November 29, 1993.

[2] A copy of claim 5, which was omitted from the appendix to Appellants' brief, appears at page 6 of the Answer.

rejected claims and thus recite allowable subject matter (Answer at 1[3]). Claims 1 and 2 have been canceled. We reverse.

The invention relates to an adder that can be used to operate in parallel on a plurality of sub-words. Figure 1 shows two N-bit operands 12 (X) and 14 (Y) each having two sub-words (17-20) for processing by adder 10, which outputs a result word 16 (Z) having two sub-words 21 and 22. Figure 2 shows a pair of single-bit adders 31 and 32 separated by a blocking circuit 33, which prevents a carry if the masking signal M_k indicates that these two adders are located on opposite sides of the boundary separating two sub-words (Spec. at 5, line 18, to 6, line 14). Figure 3 shows a 4-bit adding section 100 having multiplexers 121-124 which permit the sum bits (e.g., S_q) of the resultant sum signal to be selectively effectively shifted by one bit position in order to divide the sum signal by two, i.e., to achieve averaging. Referring to multiplexer 122, for example, when the averaging signal A is true, the multiplexer provides bit S_{q+3} as output bit Z_{q+2}; when the averaging signal is false, the multiplexer provides sum bit S_{q+2} as output bit Z_{q+2} (Spec. at 9, lines 1-5). When a shift occurs (i.e., when average signal A is

[3] We note, however, that these claims are now in independent form and thus not properly objected to (Answer at 1) for depending on rejected base claims.

true), multiplexer 121 for the most significant bit position provides the carry signal C_{q+3} as output Z_{q+3} (Spec. at 9, lines 13-15). The disclosed circuitry can also be used to subtract sub-words and divide the result by two (see claim 5).

The references relied on by the examiner are:

Gerrath	4,789,953	Dec. 06, 1988
Patti et al. (Patti '975)	5,047,975	Sep. 10, 1991
Patti et al. (Patti '636)	5,189,636	Feb. 23, 1993

A. The rejection of claim 5

Claim 5 reads as follows:

5. An apparatus for operating on the contents of an X word having bits X_i and a Y word having bits Y_i to generate a result word having bits Z_i, where i=0 to N-1, where Z_0 is the least significant bit of one of said sub-words and Z_{N-1} is the most significant bit of one of said sub-words, said apparatus comprising:

means for partitioning said X, Y and result words into a plurality of sub-words, there being one sub-word of said Y and result words corresponding to each sub-word of said X word;

means, responsive to a first instruction, for generating the sum of each X sub-word and the corresponding Y sub-word, the result thereof determining said corresponding sub-word of said result word; and

means, responsive to a second instruction, for generating the difference of each sub-word in said X word and the corresponding sub-word in said Y word, the result thereof determining said corresponding sub-word of said result word; and

means, responsive to a third instruction, for generating the difference divided by two of each sub-word in said X word and the corresponding sub-word in said Y word, the result thereof determining said corresponding sub-word of said result word.

Claim 5 stands rejected under 35 U.S.C. § 103 as unpatentable for obviousness over the adder shown in Figure 4B of Patti '975 or Patti '636.[4] This adder, which includes two 8-bit adder circuits 450 and 452, is selectively operated to perform either a conventional ADD operation or a dual-add-with saturate operation (Patti '975, col. 15, lines 38-43) in order to accommodate video signals in either of two different formats. Specifically, when the SPLIT signal is false, the adder is used to sum two conventional 16-bit two's complement values A and B, with the eight least significant bits (8LSB) being summed in adder circuit 452, the eight most significant bits (8LSB) being summed in adder circuit 450, and the carry-out terminal CO_0 of adder circuit 452 being connected by AND gate 454 to carry-in terminal CI_1 of adder circuit 450. On the other hand, when SPLIT is true, the adder is used to sum two input words each having an 8-bit sub-word representing an unsigned binary value and another 8-bit sub-word representing an 8-bit offset-128 value (col. 16, lines 13-26). More particularly, the modified sum produced by each 8-bit adder circuit is an 8-bit unsigned binary value representing the sum of the input 8-bit unsigned binary value and

[4] While Patti '636 is a continuation-in-part of Patti '975, the examiner relies only on commonly disclosed subject matter.

the input 8-bit offset-128 binary value (col. 16, lines 8-13). Also, when SPLIT is true, the AND gate 454 is disabled, thereby disconnecting carry-out terminal CO_0 of adder circuit 452 from carry-in terminal CI_1 of adder circuit 450. Appellants concede (Brief at pages 3-4) that

> given two operands X and Y, the X operand being divided into sub-operands X1 and X2 and the Y operand being dividable into sub-operands Y1 and Y2, the device taught by Patti, *et al.* computes either $[X_1 \pm Y_1]$ and $[X_2 \pm Y_2]$ or $X \pm Y$. The choice of whether the sums or differences are performed or whether partial word or whole word operations are performed is determined by the specific instruction.

The examiner agrees with Appellants that the Patti references do not disclose "means, responsive to a third instruction, for generating the difference divided by two of each sub-word in said X word and the corresponding sub-word in said Y word, the result thereof determining said corresponding sub-word of said result word." The examiner maintains that this

> feature is old and well known in the art. Moreover, the common knowledge and common sense of the person of ordinary skill in the art at the time the invention was made to use the "difference divided by two" in . . . Patti et al.'s adder. [Answer at 3.]

The examiner additionally relies on the "well known fact in the digital computing art that to enable 'divided by two' to be performed more quickly, a shifter could be used to perform the desired function" (Answer at 5).

Appellants do not dispute that it was known in the art to use a shifter to effect division by two. Instead, they argue (Brief at 4) that (1) the examiner has not pointed to any suggestion in the Patti references that would have caused one of ordinary skill in the art to alter the system taught therein so as to arrive at the present invention, (2) the examiner has failed to appreciate that "circuitry must be provided at each sub-operand boundary to assure that the overflow output of the adding stage at the most significant bit boundary is routed to the most significant bit of the corresponding partial operand after the shift," and (3) the Patti references do not teach the computation of $[X_1 \pm Y_1]/2$ and $[X_2 \pm Y_2]/2$ in a single instruction.

We agree with Appellants on the first point and therefore need not reach the other two. The examiner has not explained, and it is not apparent to us, why one skilled in the art, knowing that a shifter can be used to effect division by two, would have been motivated to use bit shifting in Patti's adder in order to generate the difference divided by two between the corresponding 8-bit sub-words of the A and B input values. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." In re Bond, 910 F.2d

831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990) (quoting Carella v. Starlight Archery and Pro Line Co., 804 F.2d 135, 140, 231 USPQ 644, 647 (Fed. Cir. 1986)). Nor has the examiner explained how Patti's adder would be modified to incorporate this feature. The rejection of claim 5 for obviousness over Patti '975 or Patti '636 is therefore reversed.

B. The rejection of claims 3, 6-14, and 16-20

The only independent claims in this group of rejected claims are claims 3 and 14. In contrast to claim 5, which as noted above, recites means responsive to an instruction for generating the difference divided by two of each sub-word in said X word and the corresponding sub-word in said Y word, claim 3 recites means responsive to an instruction for generating the sum divided by two of each sub-word in said X word and the corresponding sub-word in said Y word. Claim 14 does not recite sub-words, instead reciting means for generating a sum in response to an average instruction and means for shifting the sum.

The examiner, noting that the Patti references do not disclose "the claimed 'sum divided by two' (claim 3) and 'means for shifting' (claim 14)," states that these features are well known in the art and that Gerrath shows an adder 8 and a shifter 13 which correspond to these features. More particularly, the

examiner contends that it would have been obvious to use Gerrath's adder 8 and shifter 13 in Patti's adders "because these features are well-known in the data processing device" (Answer at 3-4). According to the examiner, Gerrath discloses "sum divided by two" in the equations at column 3, line 40 (Answer at 4-5).

We agree with Appellants that the examiner's reliance on Gerrath's adder 8 and shift register 13 is misplaced. Gerrath's adder 8 is part of a circuit that calculates an output value Y_n in accordance with the formula $Y_n=Y_{n-1}(1-\alpha)+\alpha X_n$, where X_n is the current value of the input signal at time t_n, α is a factor which determines the transient response of the filter, and Y_{n-1} is the output value calculated at time t_{n-1} (col. 1, lines 55-63). Furthermore, as shown in Figure 1, one output value (Y_{n1}, Y_{n2}, Y_{n3}, etc.) is calculated for each interval between transitions of the input waveform X. At each transition of the input waveform, the output value Y_n for the preceding interval is entered into shift register 13, which has a number of stages equal to the number of transitions in one period of the input waveform or a multiple of one period of the input waveform (col. 5, lines 1-10). The output values Y_n which are currently stored in the shift register are combined in an adder to form an arithmetic sum of those output values, which sum is divided in divider stage 15 by a

number equal to the number of stages in shift register 13 to produce a value representing a moving average of the output values (col. 1, lines 41-53). Thus, as Appellants correctly note, Gerrath's adder 8 and shift register 13 do not perform a sum-divided-by-two function, as alleged by the examiner, with the result that Gerrath fails to suggest modifying Patti in a way that satisfies claim 3 or claim 14. Nor has the examiner explained why one skilled in the art, knowing that a shifter can be used to effect division by two, would have been motivated to use bit shifting in Patti's adder in order to generate the sum divided by two of the corresponding 8-bit sub-words of the input values A and B (which would satisfy claim 3) or in order to shift the sum of the 16-bit input values A and B (which would satisfy claim 14).

For the foregoing reasons, the rejection of claims 3 and 14 and their dependent claims 6-13 and 16-20 under 35 U.S.C. § 103 for obviousness over either of the Patti patents in view of Gerrath is also reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)
JOHN C. MARTIN Administrative Patent Judge	) BOARD OF PATENT)) APPEALS AND)) INTERFERENCES
JAMES T. CARMICHAEL Administrative Patent Judge	)

Records Manager
Legal Department, 20B0
Hewlett-Packard Company
P. O. Box 10301
Palo Alto, CA 94303-0890